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KS152JB Status Update and Background

The KS152JB is the part designation for KLSI's design, which is intended to be a replacement for the Intel 80C152JB-1. Intel discontinued the 80C152Jx family in 1998. The KS152JB design went into initial production in mid 1999 after sampling and testing by early involvement customers in late 1998 and early 1999.

The basic features of this device are briefly described here. For a more detailed description consult the Intel 80C152 Technical Manual.

Basic functions:

- **80C51 8 bit u controller + 256 bytes RAM**
- **7 - 8 bit I/O Ports (multi-purpose, programmable)**
- **Multi-protocol Comm Channel (GSC)- Global Serial Channel**
  - **Supported Functions: CSMA/CD , SDLC/HDLC , or User defined**
- **MCS -51 type UART (LSC)- Local Serial Channel**
- **2 - DMA channels**
- **2 - GP Counters/Timers**
- **11 Interrupt Sources**

This list of 80C152 functions is presented only to highlight that the device is a fairly complex part, with many interacting modes of operation. In developing the KLSI version, only publicly available documentation and internal interpretation of correct operation of the device was used. There was no "formal verification" or "Design verification" baseline to insure absolute Intel 80C152 behavior in all cases. Consequently, final verification is by the end user evaluating the design in their final product environment with their application software.

Design Status

There are at present 2 versions of the part: KS152JB3 and KS152JB4

KS152JB3 - This part was first tested, approved, and shipped to the first customers in early 1999. Subsequent customers have found the following problems:

UART: (LSC) , MCS-51 type UART. - In all modes except mode 0, the UART has a small timing window where it can miss the START bit and ignore the sent character.

Impact: The UART is "OK" for local keyboard, debug mode, but cannot be relied on for correct record or file transfer, except in Mode 0.

HDLC: (GSC) , full duplex mode operation. - In HDLC, full duplex mode, the TRANSMITTER will wait until the RECEIVER is "quiet" before starting to send. Upstream sends of an "IDLE state/FLAG" signal will stall a network loop setup to send idle flags when waiting, as opposed to "all zero" idle.

KS152JB4 - This part fixes the above problems and reduces the device power to be more in line with the Intel part.

At this time information from customer tests indicate the fixes work. For other users, we are working to confirm some new found differences in the CSMA back-off algorithm or PRN counter for collision retry and some HOLD/HOLDA differences in DMA operation. It is unknown if these problems are in the JB3 device.