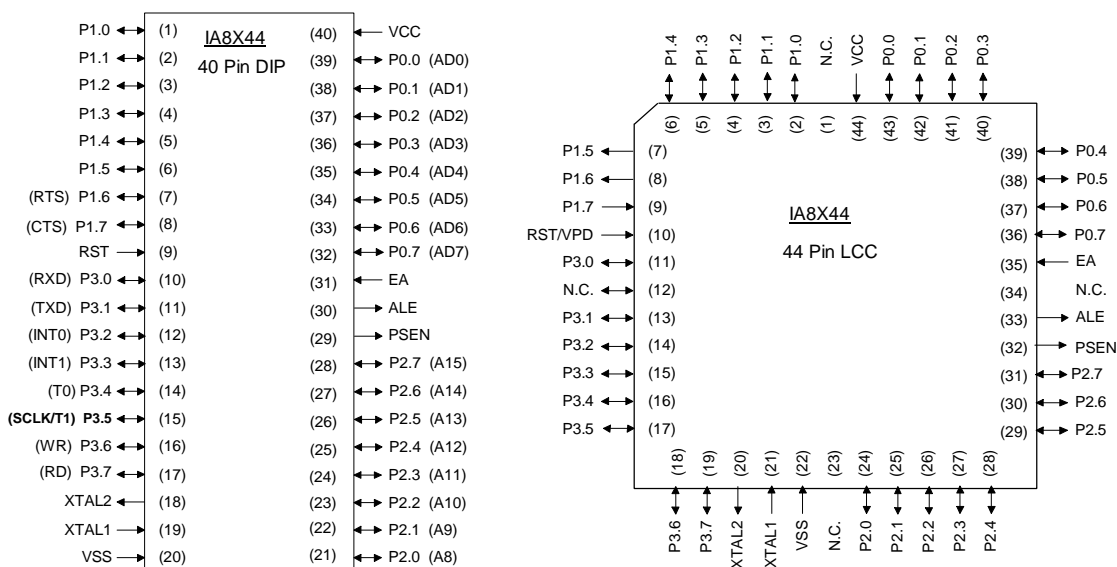


IA8X44**SDLC COMMUNICATIONS CONTROLLER****Advanced Information Sheet****FEATURES**

- **Form, Fit, and Function Compatible with the Intel[®] 8X44**
- **Packaging options available: 40 Pin Plastic or Ceramic DIP, 44 Pin Plastic Leaded Chip Carrier**
- **8-Bit Control Unit**
- **8-Bit Arithmetic-Logic Unit with 16-Bit multiplication and division**
- **12 MHz clock**
- **Four 8-Bit Input / Output ports**
- **Two 16-Bit Timer/Counters**
- **Serial Interface Unit with SDLC/HDLC compatibility**
- **2.4 Mbps maximum serial data rate**
- **Two Level Priority Interrupt System**
- **5 Interrupt Sources**
- **Internal Clock prescaler and Phase generator**
- **192 Bytes of Read/Write Data Memory Space**
- **64kB External Program Memory Space**
- **64kB External Data Memory Space**
- **4kB Internal ROM (ia8044 only)**

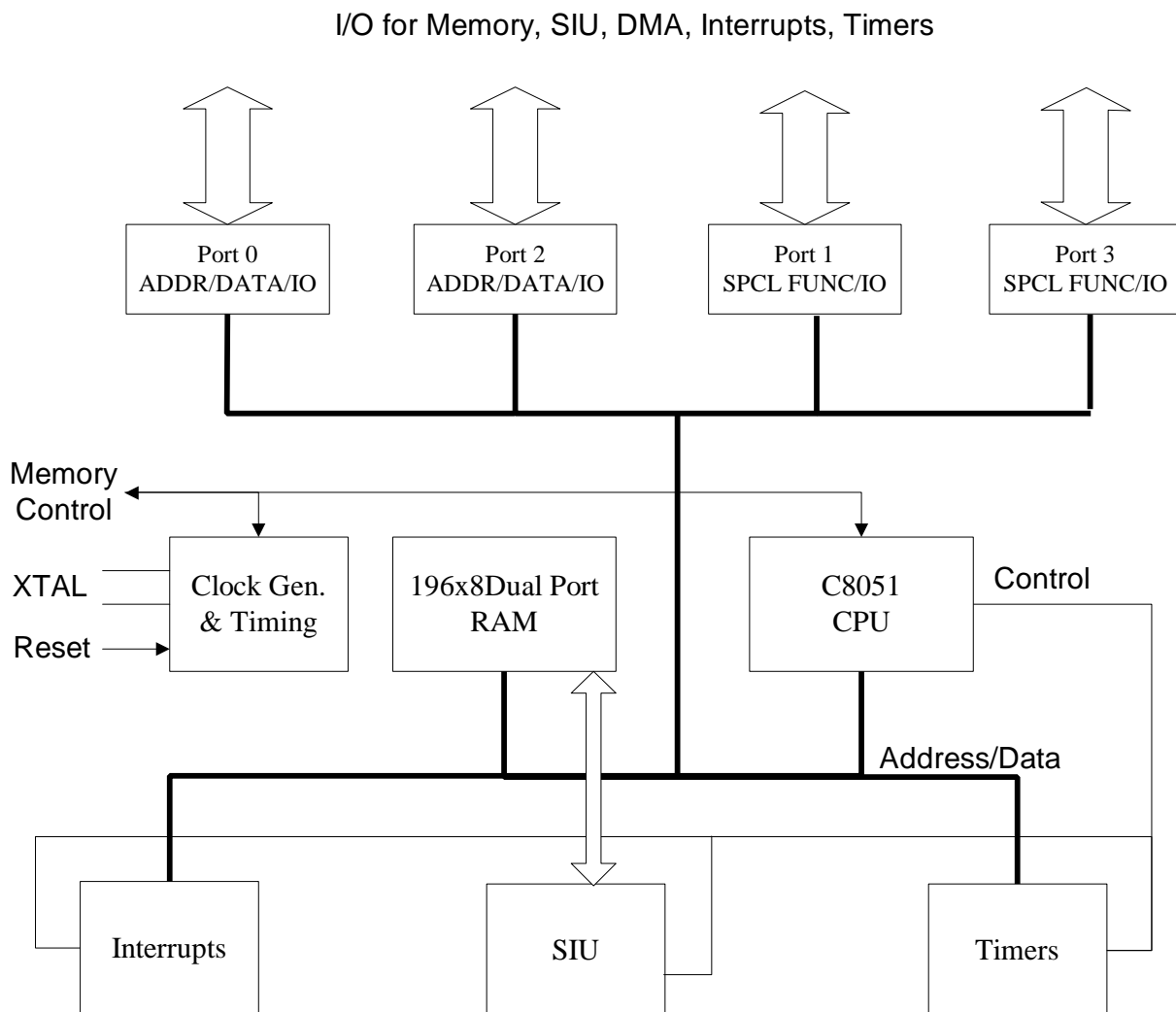
The IA8X44 uses **innovASIC**'s innovative new **f³ Program** to provide industry with parts that other vendors have declared obsolete. By specifying parts through this program a customer is assured of never having a component become obsolete again. This advanced information sheet assumes the original part has been designed in, and so provides a summary of capabilities only. For new designs contact **innovASIC** for more detailed information.

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IA8X44**Advanced Information Sheet****SDLC COMMUNICATIONS CONTROLLER**

The IA8X44 is a form, fit and function compatible part to the Intel 8X44 SDLC communications controller. The IA8x44 is a Fast Single-Chip 8-Bit Microcontroller with an integrated SDLC/HDLC serial interface controller. The IA8X44 is a fully functional 8-Bit Embedded Controller that executes all ASM51 instructions and has the same instruction set as the Intel 80C51. The IA8X44 can access the instructions from two types of program memory, serves software and hardware interrupts, provides an interface for serial communications and a timer system. The IA8X44 is fully compatible with the Intel 8X44 series. A block diagram is shown in Figure 1.

Functional Block Diagram**Figure 1**

SDLC COMMUNICATIONS CONTROLLER

I/O Signal Description

Table 1 below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provided. Table 2 refers to the variants between the IA8044 and the IA8344. Environmental/Qualification Levels are listed in Table 3.

I/O Characteristics

Table 1

Name	Type	Description
RST	I	Reset. This pin when held high for two machine cycles while the oscillator is running will cause the chip to reset.
ALE	O	Address Latch Enable. Used to latch the address on the falling edge for external memory accesses.
PSEN	O	Program Store Enable. When low acts as an output enable for external program memory.
EA	I	External Access. When held low EA will cause the ia8X44 to fetch instructions from external memory.
P0.7 – P0.0	I/O	Port 0. 8 bit I/O port and low order multiplexed address/data byte for external accesses.
P1.7 – P1.0	I/O	Port 1. 8 bit I/O port. Two bits have alternate functions, P1.6 (RTS) and P1.7 (CTS).
P2.7 – P2.0	I/O	Port 2. 8 bit I/O port. It also functions as the high order address byte during external accesses.
P3.7 – P3.0	I/O	Port 3. 8 bit I/O port. Port 3 bits also have alternate functions as described below. P3.0 – RXD. Receive data input for SIU or direction control for P3.1 dependent upon datalink configuration. P3.1 – TXD. Transmit data output for SIU or data input/output dependent upon datalink configuration. Also enables diagnostic mode when cleared. P3.2 – INT0. Interrupt 0 input or gate control input for counter 0. P3.3 – INT1. Interrupt 1 input or gate control input for counter 1. P3.4 – T0. Input to counter 0. P3.5 – SCLK/T1. SCLK input to SIU or input to counter 1. P3.6 – WR. External memory write signal. P3.7 – RD. External memory read signal.
XTAL1	I	Crystal Input 1. Connect to VSS when external clock is used on XTAL2.
XTAL2	O	Crystal Input 2. Can connect to a crystal or external clock.
VSS	P	Ground.
VCC	P	+5V power.

IA8X44 Advanced Information Sheet

SDLC COMMUNICATIONS CONTROLLER

IA8X44 Variants

Table 2

IA8044	4kB internal ROM with R0177 version 2.1 firmware, 192 byte internal RAM (Expandable to 256 Bytes), 64kB external program and data space.
IA8344	192 byte internal RAM, 64kB external program and data space.

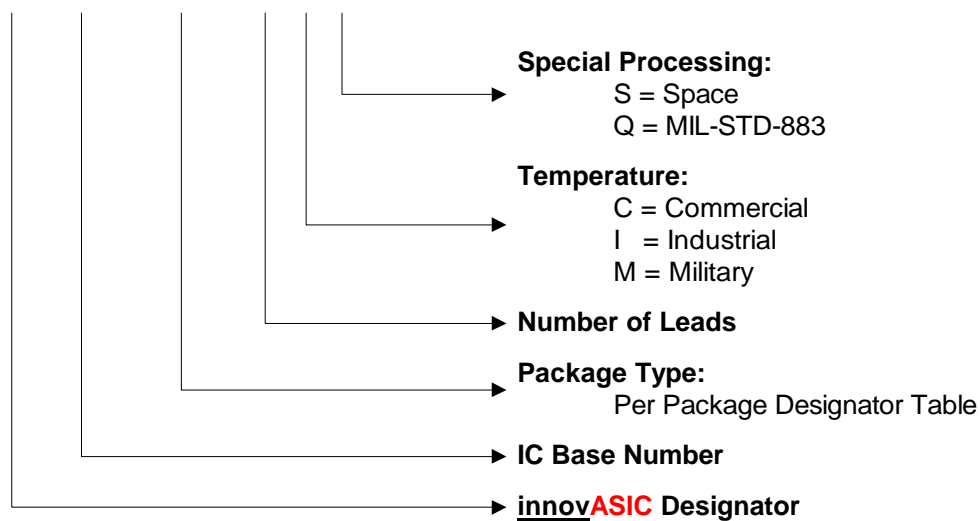
Qualification Levels

Table 3

Part Number	Environmental/ Qual Level
IA8044-PDW40I	Industrial
IA8044-PLC44I	Industrial
IA8344-PDW40I	Industrial
IA8344-PLC44I	Industrial

The following diagram depicts the **innovASIC** Product Identification Number.

IAXXXXX-PPPPNNT/SP



SDLC COMMUNICATIONS CONTROLLER

Package Designator Table

Package Type	innovASIC Designator
Ceramic side brazed Dual In-line	CDB
Cerdip with window	CDW
Ceramic leaded chip carrier	CLC
Cerdip without window	CD
Ceramic leadless chip carrier	CLL
PLCC	PLC
Plastic DIP standard (300 mil)	PD
Plastic DIP standard (600 mil)	PDW
Plastic metric quad flat pack	PQF
Plastic thin quad flat pack	PTQ
Skinny Cerdip	CDS
Small outline plastic gull-wing(150 mil body)	PSO
Small outline medium plastic gull-wing (207 mil body)	PSM
Small outline narrow plastic gull wing (150 mil body)	PSN
Small outline wide plastic gull wing (300 mil body)	PSW
Skinny Plastic Dip	PDS
Shrink small outline plastic (5.3mm .208 body)	PS
Thin shrink small outline plastic	PTS
Small outline large plastic gull wing (330 mil body)	PSL
Thin small outline plastic gull-wing (8 x 20mm) [TSOP]	PST
PGA	CPGA
BGA	CBGA

Contact **innovASIC** for other package and processing options.